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SG			Fu, C., et al., "Value Speculation Scheduling for High Performance Processors", <u>ASPLOS VII</u> , pp. 262-271, (1998)			
SG			Lipasti, M.H., et al., "Value Locality and Load Value Prediction", <u>ASPLOS VII</u> , pp. 138-147, (1996)			
SG			Luk, C., "Tolerating Memory Latency through Software-Controlled Pre-Examination in Simultaneous Multithreading Processors", <u>IEEE/ISCA</u> , 12 p., (2001)			
SG			Purser, Z., et al., "A Study of Slipstream Processors", <u>IEEE/ACM Int'l. Symp. on Microarch., Proc. 33rd Annual</u> , pp. 269-280, (2000)			
SG			Wang, K., et al., "Highly Accurate Data Value Prediction", <u>IEEE/ACM Int'l Symp. on Micro Arch., Proc. 30th Annual</u> , pp. 358-363, (1997)			
SG			Zilles, C., et al., "Execution-based Prediction using Speculative Slices", <u>IEEE/ISCA</u> , 12 p., (2001)			
SG			Zilles, C.B., et al., "Understanding the Backward Slices of Performance Degrading Instructions", <u>ISCA Int'l Symp. of Comp. Architecture</u> , pp. 172-181, (2000)			

Examiner <i>Shane Smith</i>	Date Considered 7/19/04
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*Substitute Disclosure Statement Form (PTO-1449)

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